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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/758,970	01/09/2001	Ronnie M. Harrison	500395.02	9636

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/758,970	HARRISON, RONNIE M.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *57-90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *84-87 and 90* is/are allowed.

6)☒ Claim(s) *57-72,76-83,88 and 89* is/are rejected.

7)☒ Claim(s) *73-75* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/30/01, 8/02/01, 9/17/01, 6/10/02, 7/30/02, 10/04/02, 5/11/03, 8/05/03, 11/24/03, 4/02/04, 12/1/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 73 is objected to because of the following informalities: in the last line, ";" should be changed to --.--. Appropriate correction is required.

2. Claim 78 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Apparatus claim 78 cannot further define a method for providing a plurality of clock signals that have predetermined phases relative to a master clock signal in claim 77.

Specification

3. The disclosure is objected to because of the following informalities: above line 5, -- This application (claims priority to) is a continuation of serial No. 08/879,847 filed on June 20, 1997; now US Patent 6,173,432. -- should be inserted.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 58-60, 76, 78, 80, 81, 88, and 89 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 58 is indefinite because the limitation "the reference clock signal is locked to the same phase as the master clock signal" is unclear. Insofar as understood, the recited limitation "A method of generating a sequence of clock signals", in base claim 57, refers to 200 in Fig. 3. Therefore, it is not clear how the above recited limitation reads on the preferred embodiment. Furthermore, the recited limitations "a first of the plurality of clock signals has the same phase as the master clock signal, a second of the plurality of "generating a first signal during the period that the phase of the master clock signal lags the phase of the one of the clock signals in the sequence; generating a second signal during the period that the phase of the master clock signal leads the phase of the one of the clock signals in the sequence; and generating as the control signal a voltage that increases toward one polarity responsive to the first signal and toward the opposite polarity responsive to the second signal" in claim 76; "producing the first/second control signal comprises: generating an enable signal during the period that the phase of the master clock signal lags the phase of the reference signal; and generating as the first control signal a voltage that increases toward one polarity responsive to the enable signal and toward the opposite polarity responsive to the absence of the enable signal" in claims 80, 81, 88, and 89; have similar problems.

Claim 78 recites the following limitations: " the first and second locked loops " in line 1; " the first signal generator " in line 2; and " the second signal generator " in line 4. There is insufficient antecedent basis for these limitations in the claim.

Claims 59-60 are rendered indefinite by the deficiencies of base claim 58.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claim 78 is rejected under 35 U.S.C. 101, as being directed to neither an "apparatus" nor a "method", but rather embraces or overlaps two different statutory classes of invention set forth in 35 U.S.C. 101.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

9. Claims 57-72, 77, 79, 82, and 83, are rejected under 35 U.S.C. 102(e) as being anticipated by Miller et al. (US Pat. 5,712,883).

With regard to claim 57, Miller et al. discloses in Figs. 1-3 an inherent method of generating a sequence of clock signals, comprising a step of delay locking a reference clock signal (18(2)) to a master clock signal (18(1)) so that the reference clock signal has a predetermined phase relative to the phase of the master clock signal; and a step of delay locking a plurality of clock signals to the reference clock signal so that the plurality of clock signals (CLK(K) through CLK(K+1)) have respective phases relative to the phase of the reference clock signal.

With regard to claims 58-60, the reference also meets the recited limitations in these claims (see Fig. 3).

With regard to claim 61, Miller et al. discloses in Figs. 1-3 an inherent method of generating a sequence of clock signals from a master clock signal (18(1)), comprising a step of generating the sequence of clock signals (CLK(K) through CLK(K+1)) each of which has a respective phase that increases from a first clock signal (CLK(K)) to a last clock signal (CLK(K+1)) in the sequence; a step of delay locking the first clock signal and last clock signals to each other so that they have a predetermined phase with respect to each other; a step of delay locking one of the clock signals to the master clock signal so that each of the clock signals in the sequence have respective phases with respect to the master clock signal.

With regard to claims 62-65, the reference also meets the recited limitations in these claims (see Fig. 3).

With regard to claim 66, Miller et al. discloses in Figs. 1-3 an inherent method of generating a sequence of clock signals, comprising a step of generating the sequence of clock signals (CLK(K) through CLK(K+1)) which are increasingly delayed from a first

clock signal to a last clock signal, two of the clock signals in the sequence being delay locked to each other so that they have a predetermined phase with respect to each other; and a step of delay locking one of the clock signals to a master clock signal (18(1)) so that the clock signals in the sequence have respective phases with respect to the master clock signal.

With regard to claims 67-72, the reference also meets the recited limitations in these claims (see Fig. 3).

With regard to claim 77, Miller et al. discloses in Figs. 1-3 an inherent method for providing a plurality of clock signals (CLK(K) through CLK(K+1)) that have predetermined phases relative to a master clock signal (18(1)), the method comprising the step of producing a reference clock signal (18A(2)), having a phase relative to the master clock signal that is a function of a first control signal (VPLL); the step of generating the first control signal as a function of the difference in phase between the master clock signal and the reference clock signal; the step of producing the plurality of clock signals having respective phases relative to the reference clock signal that are a function of a second control signal (VPLL); and the step of generating the second control signal as a function of the difference in phase between the reference clock signal and one of the plurality of clock signals.

With regard to claims 79, 82, and 83, the reference also meets the recited limitations in these claims (see Figs. 3-5).

Allowable Subject Matter

10. Claims 73-75 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a method of generating a sequence of clock signals (264a through 264n in instant Fig. 3) comprising the specific steps, as recited in claim 73, such as the step of receiving a reference clock signal (256); generating the sequence of clock signals from the reference clock signal by the step of delaying the reference clock signal by respective delays (260) that are a function of a control signal (270); and the step of comparing (330) the phase of two of the clock signals (264a, 264n) in the sequence and the step of generating (272) the control signal as a function of the difference therebetween; and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a method of generating a sequence of clock signals (264a through 264n in instant Fig. 3) comprising the specific steps, as recited in claim 75, such as the step of delay locking (252, 254, 260, 290, 292) one of the clock signals to a master clock signal comprises the step of receiving the master clock signal (A); the step of generating (252) a reference clock signal (256) having a delay relative to the master clock signal that is a function of a control signal (258); and the step of comparing (330) the phase of the master clock signal to the phase of one (264n) of the clock signals in the sequence and the step of generating the control signal as a function of the difference therebetween; and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

11. Claims 84-87 and 90 are allowed.

The prior art of record fails to disclose or fairly suggest a method of generating a sequence of clock signals that have predetermined phases relative to a master clock signal, as recited in claim 84, comprising the specific steps such as the step of generating a reference clock signal (256 in instant Fig. 3) having a delay relative to the master clock signal (42) that is a function of a first control signal (258); generating the sequence of clock signals (264a through 264n) each of which has a delay relative to an adjacent clock signal in the sequence that is a function of a second control signal (270); comparing (272) the phase of two of the plurality of clock signals (264a, 264n) and generating the second control signal as a function of the difference therebetween; and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

Conclusion

12. Regarding claims 58-60, 76, 80, 81, 88, and 89, the patentability thereof cannot be determined because of their indefiniteness.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Leung et al. (US Pat. 5,485,490) is cited as of interest because it discloses a method and circuitry for clock synchronization circuit.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
December 2, 2004

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